The scanning procedure uses lines PB0 — PB5 of the PIA, corresponding to SCNREG in the JBUG assembly listing. The digit patterns to be displayed are put out on lines PA0 — PA6 and are designated as DISREG in the listing. The JBUG monitor program alternates between refreshing the display and checking for a key closure in the following manner.

The OUTDS subroutine places the digit pattern for the left-most display on PA0 — PA6 and then sets PB5 high, causing that digit to be lighted. During this time, PB4 — PB0 are low, thus the other digits are off. This digit of the display is held on for approximately 1.0 ms, after which the pattern for the second digit is put on lines PA0 — PA6. PB5 is switched low, and PB4 is taken high to select the second digit. This sequence continues until the right-most digit has been selected, at which time the program goes to the KEYDC subroutine to check for key closures. The blanking pattern ($FF) is placed on PA0 — PA6 to blank the display so that lines PB0 — PB5 can be used to interrogate and decode the keyboard. Following the keyboard check, operation returns to the display sequence. The refresh rate is fast enough that the displays appear to be on continuously.

An MC14539 CMOS One-of-Four Data Selector (U10) is used to sequentially select each column in the keypad matrix and route it to PA7 for testing by the monitor program. The address data for selecting each column is output to the Data Selector on lines PB6 and PB7. Refer to the description of the monitor program in Section 3-4 for details of the keyboard decoding technique. Note that CB1, a PIA interrupt input, is directly connected to column 2. This allows the E key to be used for generating an $\overline{\text{NMI}}$ interrupt for escaping from "blown" user programs. The MC75452 buffers serves to increase the PIA's drive capability.

2-6 TRACE (EXECUTE SINGLE INSTRUCTION)

A hardware trace function is provided that permits a user's program to be executed one instruction at a time. Results of the execution, including MPU Register contents, can be examined between each Trace command. The Trace function will operate on programs in either RAM or ROM and is useful as a debugging aid. The circuitry consists of an MC8316 Counter and two MC7479 D-flip-flops connected as shown in Figure 2-6-1. Refer to this figure also for the associated timing waveforms.

When a Trace command occurs, the system is normally in the Register display mode from either a previous Trace or having run to a Breakpoint. Thus, the user's Register values are stacked and the monitor program is alternating between refreshing the displays and checking for new key closures. The user Program Counter value saved on the stack is pointing to the next user instruction to be executed. Invoking a Trace command at this point causes the MPU to start the Trace Counter (via CA2 of the Keyboard/Display PIA) and then execute a Return from Interrupt (RTI) instruction. This causes the MPU to reload its Registers from the stack and begin executing the next user instruction. In the meantime the Trace counter is counting machine cycles. The eleventh cycle after the counter is started will be a fetch of the op-code for the next user instruction (RTI takes ten cycles to execute). The Trace circuitry detects the eleventh cycle and generates a low going $\overline{\text{NMI}}$ signal. Since the shortest instruction is at least two cycles long, $\overline{\text{NMI}}$ will always be low at the end of the first instruction and will cause a return to the JBUG monitor program via an $\overline{\text{NMI}}$ interrupt. The $\overline{\text{NMI}}$ service routine sets CA2 back high, resetting the counter in readiness for another command. The $\overline{\text{NMI}}$ service routine is described in Section 3-8 in greater detail. From the user's point of view, closure of the N (Trace) key causes the system to execute one instruction and then stop so that the results can be examined.

2-7 AUDIO CASSETTE INTERFACE

Circuitry for interfacing an ACIA to an audio cassette recorder/player is included on the Keyboard/Display Module. This circuitry enables the user to store and retrieve data on ordinary audio cassettes at a 300

baud (30 characters per second) serial clock rate. Data is stored on the tape using the ''Kansas City Standard'' recording format, so-called due to its formulation during a symposium sponsored by *BYTE* Magazine in Kansas City, Missouri in November, 1975. The format is designed to eliminate errors due to audio system speed variations[5] and has the following characteristics:

1. A Mark (logical one)[6] is recorded as eight cycles of a 2400 Hz signal.
2. A Space (logical zero) is recorded as four cycles of a 1200 Hz signal.
3. A recorded character consists of a Space as a start bit, eight data bits, and two or more Marks as stop bits.
4. The interval between characters consists of an unspecified amount of time at the Mark frequency.
5. In the data character, the least significant bit (LSB) is transmitted first and the most significant bit (MSB) is transmitted last.
6. The data is organized in blocks of arbitrary and optionally variable length preceeded by at least five seconds of Marks.
7. Meaningful data must not be recorded on the first 30 seconds of tape following the clear leader.

A control program in JBUG causes this format to be followed and incorporates the following additional characteristics:

1. At the beginning of tape (BOT), the ASCII character for the letter ''B'' is recorded following 1024 Marks (approximately 30 seconds).
2. The ''B'' is followed by one byte containing the block length (up to 256 bytes in a particular block).
3. The next two bytes recorded contain the starting address in memory from which the data is coming.
4. Up to 256 bytes of data are then recorded and followed by 25 marks and the ASCII character for the letter ''G''.

The control program uses the additional features to insure that the Punch and Dump functions are performed in an orderly manner (see the explanation in Section 3-7 for additional information).

The cassette inferface circuit diagram of Figure 2-7-1 serves as an aid to understanding the following description of the Punch and Load operations. The Punch (transfer of data from the Microcomputer Module's memory to tape) and Load (transfer from tape to memory) commands are accomplished by a combination of the control program, the MC6850 Asynchronous Interface Adapter (ACIA), and the cassette interface circuitry.

The ACIA is, in effect, a bus-oriented, universal, asynchronous receiver/transmitter (UART). In the transmit mode (Punch), it accepts parallel 8-bit data from the MPU bus, adds the formatting start bit and stop bit, and then converts the data to a serial binary stream (Tx Data in Figure 2-7-1). The desired format is established by instructions from the MPU as it executes the Punch command. In the receive mode (Load), the ACIA accepts an incoming serial data stream (Rx Data) and a sampling clock (Rx Clk). It strips off the start/stop bits and passes each incoming byte to the MPU for transfer to memory, again under control of the MPU as the

[5]The circuitry provided with the kit will accommodate speed variation of approximately ±25%.

[6]Logical ones and zeros will be alternatively referred to as Marks and Spaces, respectively, in accordance with serial data transmission conventions.

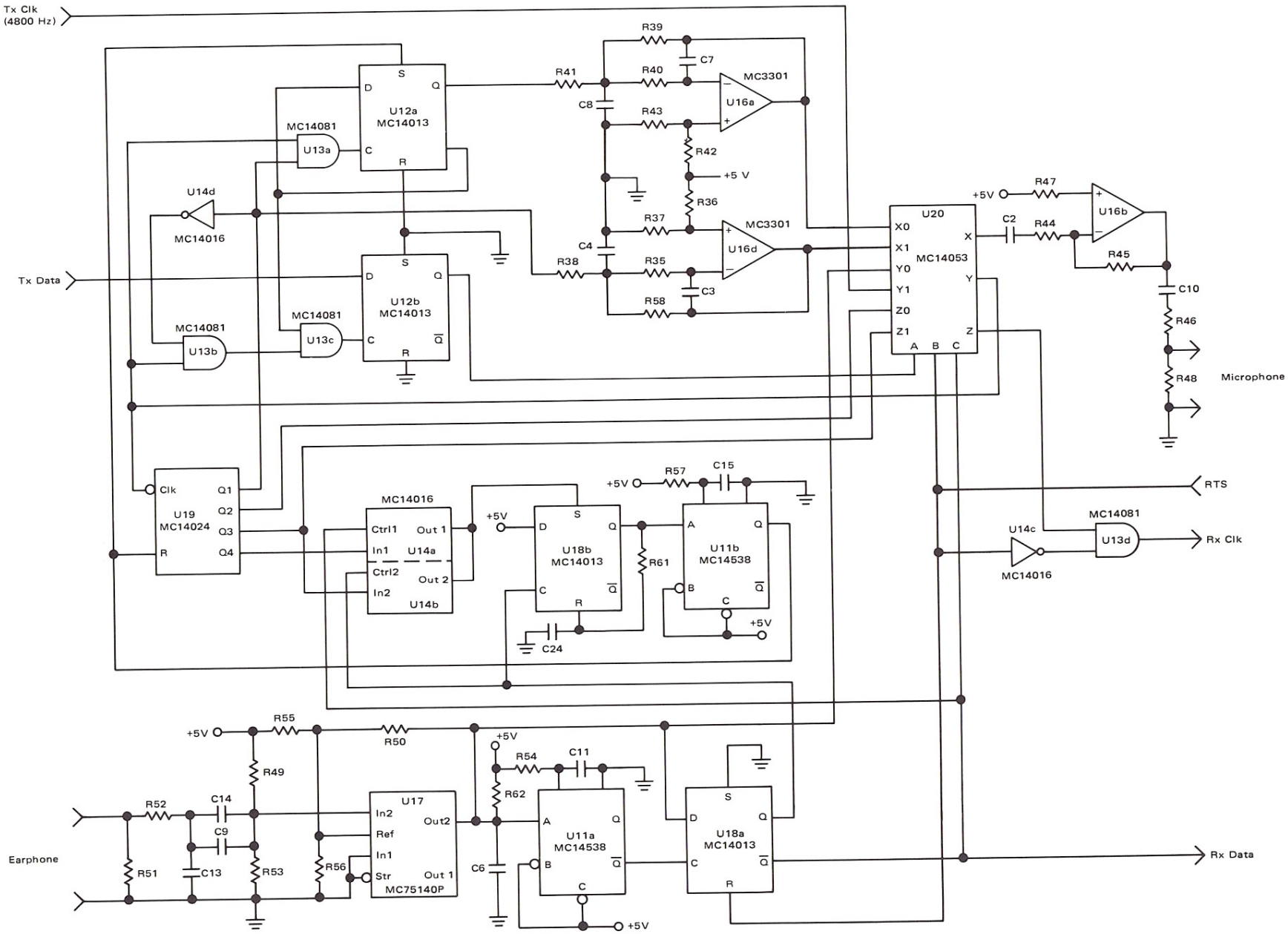

FIGURE 2-7-1. Audio Cassette Interface Circuitry

program executes. The ACIA's Request-to-Send, $\overline{\text{RTS}}$, acts as a gating signal to switch the interface circuitry between the Punch and Load modes. The reference documents may also be referred to for additional details on the ACIA's characteristics.

Timing waveforms corresponding to the appropriate signals in Figure 2-7-1 are provided as Figures 2-7-2, 2-7-3, and 2-7-4 as an aid to study of the cassette interface circuitry.

During a Punch operation the interface circuitry operates on the serial data to convert each logical one (Mark) to an 8-cycle burst of 2400 Hz signal and each logical zero (Space) to a 4-cycle burst of 1200 Hz signal which is then recorded on tape.

The circuitry reverses this procedure during a Load operation; it decodes the incoming frequency-modulated signal in order to recover the binary data and a sampling clock.

In Figure 2-7-1, the MC14053 Multiplexer/Demultiplexer, U20, (Data Router, for simplicity) is used to steer signals to their required points during both Load and Punch operations. For instance, during Punch, B and C are high while A is derived from the binary data on Tx Data. For this combination of control signals Y is connected to Y1 (because B is high); thus the 4800 Hz Tx Clk signal from the Microcomputer Module is applied to the clock input of the MC14024 Counter, U19. Also, because C is high, Z is connected to Z1, but this signal is not used during Punch. The 2400 Hz and 1200 Hz signals are obtained by selecting either the ÷2 (Q1) or the ÷4 (Q2) outputs of the Counter as it is clocked at 4800 Hz.

The signals at X0 and X1 are 1200 and 2400 Hz sine waves obtained via the bandpass filters of U16a and U16d. One or the other of these signals (depending on the Tx Data logic level at A) will be level shifted, attenuated, and applied to the microphone output terminals.

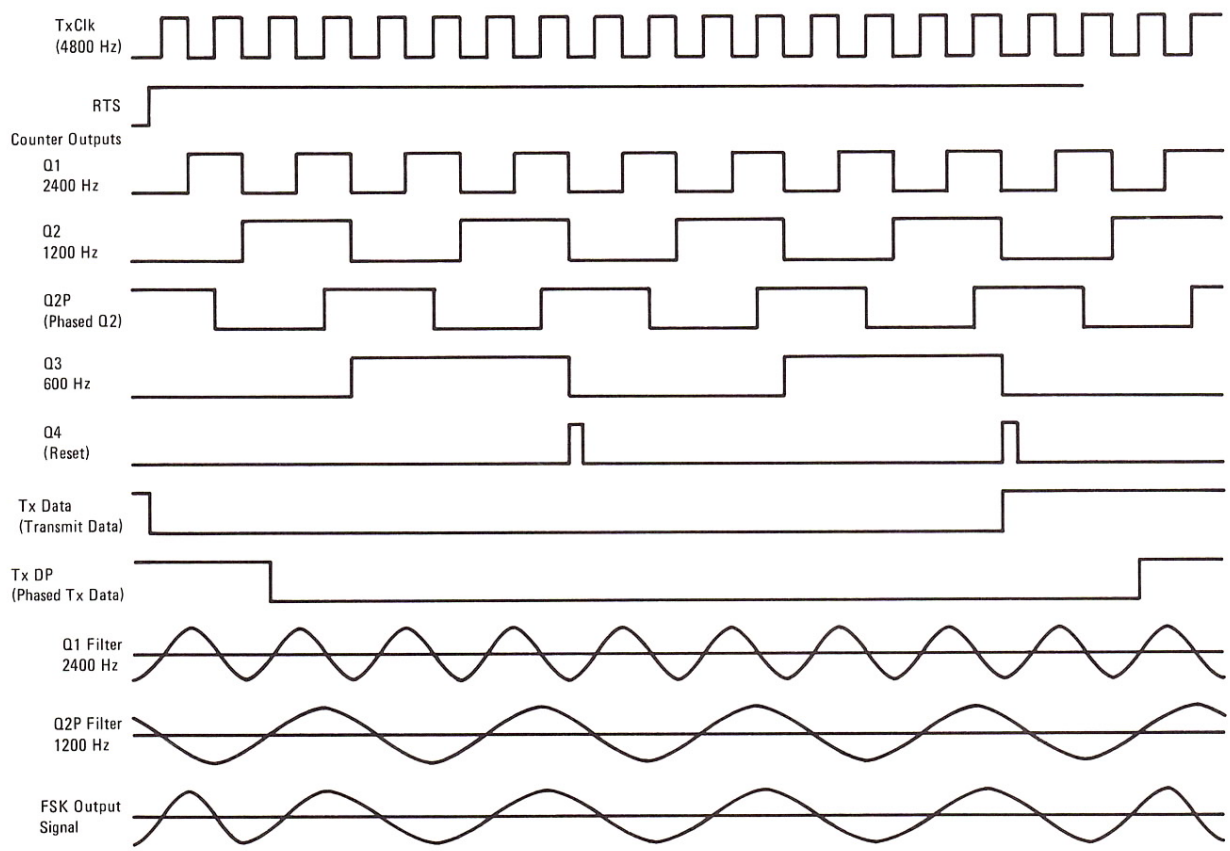

FIGURE 2-7-2. Transmit Waveforms

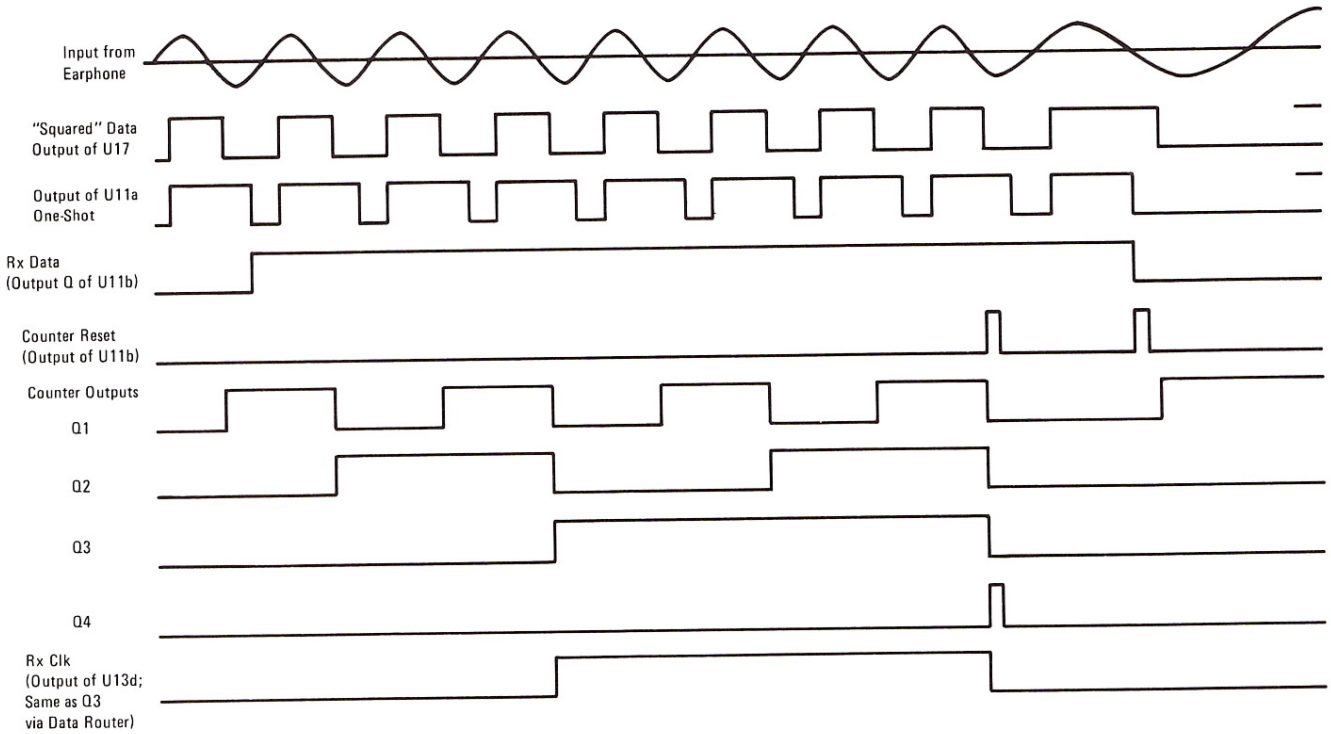

FIGURE 2-7-3. Receive Waveforms, Space-to-Mark Transition

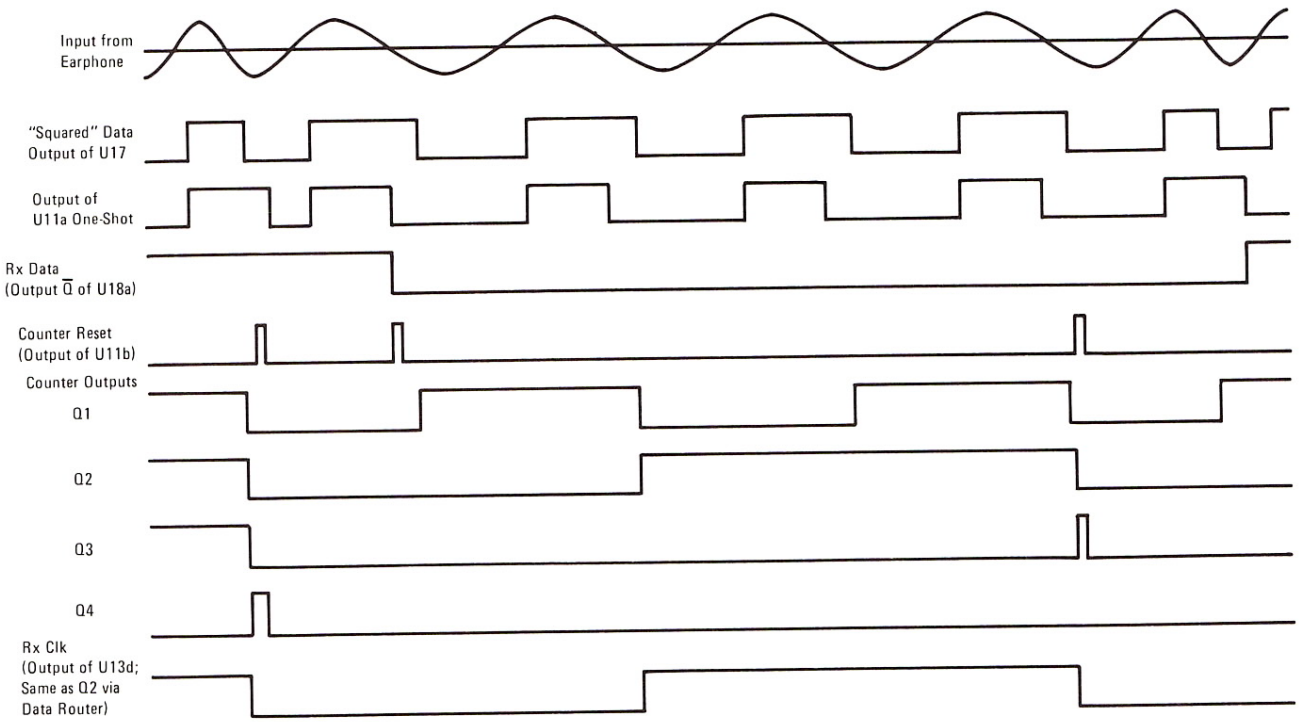

FIGURE 2-7-4. Receive Waveforms, Mark-to-Space Transition

Note that the 1200 Hz square wave is obtained from the output of U12a rather than the Q2 output of the MC14024. This, together with the gating of U13 and the delay associated with U12b, insures that switching of output frequencies will occur only when the outputs of U16a and U16d are at essentially the same voltage. (Refer to the timing diagram of Figure 2-7-2.)

During a Load operation, the incoming signal from the cassette earphone is filtered, amplified and squared by the U17 Line Receiver. (U17 is connected as a Schmitt trigger to reduce noise problems.) This results in a signal, at digital levels, that varies between 2400 Hz and 1200 Hz according to the one-zero pattern that was recorded on the tape. This frequency-modulated signal is then converted to logical ones and zeros by the pulse width discriminator formed by the U11a MC14538 Monostable Multivibrator (or One-Shot) and the U18a type D flip-flop. Incoming signals less than 1800 Hz are decoded as zeros; frequencies higher than 1800 Hz are decoded as ones. The Received Data will be present at the $\overline{Q}$ output of U18a.

The required Rx Clk signal, a positive transition at the mid-point of each bit-time and a negative transition at the end of each bit-time, is generated as follows:

During Load the digital level 2400/1200 Hz signal, instead of the 4800 Hz Tx Clk signal, is steered to the Counter clock input. The Counter's $\div 8$ (Q3) and $\div 16$ (Q4) outputs are connected to the inputs of U14b and U14a, respectively. The control inputs of U14a and b are connected to Received Data and applied to the Set input of U18b. The Output of U18b triggers the Counter Reset one-shot, U11b. Hence, either the $\div 8$ or $\div 16$ Counter output is steered back (via X) as a reset, depending on whether the data is a zero or a one, respectively. The Counter is also reset by every Mark-to-Space transition via the U11b One-Shot. The Counter's $\div 4$ and $\div 8$ outputs are connected to Z0 and Z1, respectively. These connections combined with the reset signals result in a positive transition at the Z output of the Data Router after either four cycles of 2400 Hz or two cycles of 1200 Hz. Thus, the Rx Clk (Z gated by $\overline{\text{RTS}}$) has a positive transition in the middle of each bit-time and a negative transition at the end of each bit-time.

2-8 KIT EXPANSION

Provision is made for buffering circuitry to allow the Microcomputer Module to be implemented into a larger system. The buffers and pinouts selected on the bottom edge connector are compatable with the EXORciser so its I/O and Memory Modules can be used with this kit. The direction of data flow across the data bus buffers is controlled by the MC7430 NAND gate, U7. This decoding provides for data flow off the board to the external system when there is a Memory Read Cycle at an address that is not decoded by the devices on the Microcomputer Module itself. Note that the signal $\overline{\text{RAM}}$ decodes the lowest 8K bytes of memory which are reserved for on-board memory (MCM6810's). Should the user want to assign the lowest 8K of memory addresses to off-board memory, the following changes are required:

Remove the MCM6810's decoding addresses 0000, 0080, 0010 and 0180; remove the signal $\overline{\text{RAM}}$ from pin 4 of the MC7430 and tie pin 4 to +5 V. The signal provided at the bus connector called $\overline{\text{RAM}}$ can be used on outside memory to indicate an MPU access to an address in the bottom 8K bytes of memory which now resides off the module.

Provision has been made for using a zener diode (1N4733) to generate a −5 V supply for the 2708 PROMs (if they are used) from −12 V in case this kit is operated in an EXORciser-type system which does not have −5 V available. Should −5 V be available, the zener diode and associated 68 ohm resistor can be omitted and the −5 V brought in through the bus connector.

APPENDIX 2
ASSEMBLY DRAWINGS AND PARTS LIST

MEK6800D2 Keyboard/Display Module Parts List

ITEM	NUMBER REQUIRED	DESCRIPTION	CATALOG NUMBER	DESIGNATION
1	3	Integrated Circuit: Peripheral Driver	MC75452P	U7, U8, U9
2	6	Integrated Circuit: 7Segment LED Display (Litronix or Monsanto)	Litronix DL704 Monsanto MAN72 or 74	U1 — U6
3	1	Integrated Circuit: Dual 4-Channel Data Selector	MC14539BCP	U10
4	1	Integrated Circuit: Dual Monostable Multivibrator	MC14538BCP	U11
5	2	Integrated Circuit: Dual D Flip-Flop	MC14013BCP	U12, U18
6	1	Integrated Circuit: Quad 2-Input AND Gate	MC14081BCP	U13
7	1	Integrated Circuit: Quad Analog Switch	MC14016BCP	U14
8	1	Integrated Circuit: Quad Op-Amp	MC3301P	U16
9	1	Integrated Circuit: Dual Line Receiver	MC75140P1	U17
10	1	Integrated Circuit: Seven Stage Ripple Counter	MC14024BCP	U19
11	1	Integrated Circuit: Analog Multiplexer/Demultiplexer	MC14053BCP	U20
12	7	Transistor, PNP	MPS2907	Q1 — Q7
13	1	Capacitor: 100μF, 16 volts		C1
14 √	14	Capacitor: 0.1μF		C2, C5, C9, C10, C14, C16-C23, C25
15	2	Capacitor: 0.05μF		C6, C13
16	3	Capacitor: 0.001μF		C3, C4, C24
17	3	Capacitor: 0.002μF		C7, C8, C15
18	1	Capacitor: 2400 pF Dipped Duramica		C11
19	7	Resistor: 4700 Ω, 1/4 W, 5%		R1, R4, R7, R10 R13, R16, R19
20	29	Resistor: 10 kΩ, 1/4 W, 5%		R2, R5, R8, R11, R14, R17, R20, R22-34, R46, R49, R53, R55, R56, R59, R60, R61, R57
21	7	Resistor: 68 Ω, 1/4 W, 5%		R3, R6, R9, R12, R15, R18, R21
22	2	Resistor: 27 kΩ, 1/4 W, 5%		R35, R40
23	8	Resistor: 100 kΩ, 1/4 W, 5%		R37, R38, R39, R41, R43, R47, R54, R58
24	2	Resistor: 100 Ω, 1/4 W, 5%		R48, R51
25	2	Resistor: 1000 Ω, 1/4 W, 5%		R52, R62
26	2	Resistor: 180 kΩ, 1/4 W, 5%		R36, R42
27	3	Resistor: 22 kΩ, 1/4 W, 5%		R44, R45, R50
28	24	Switch (Stackpole)	LO — PR05	S1 — S24
29	16	Keytops, Double-Shot, Molded, White (Stackpole)	Used with S1 — S24, Item 32	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F
30	8	Keytops, Double-Shot, Molded, Blue (Stackpole)		E, G, L, M, N, P, R, V
31	1	Connector Cable		
32	1	Printed Wiring Board		